Qucs

A Report

Verilog-A implementation of the EKV v2.6 long and short channel MOSFET models

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Introduction

This report presents the background to the Qucs implementation of the EKV 2.6 long and short channel MOSFET models. During 2007 the Qucs development team employed the EKV v2.6 MOSFET model as a test case while developing the Qucs non-linear equation defined devices (EDD)\(^1\). More recently complete implementations of the long and short channel EKV v2.6 models have been developed using the Qucs Verilog-A compact device modelling route. This work forms part of the Verilog-A compact device modelling standardisation initiative\(^2\). The EKV v2.6 MOSFET model is a physics based model which has been placed in the public domain by its developers. It is ideal for analogue circuit simulation of submicron CMOS circuits. Since the models introduction and development between 1997 and 1999 it has been widely used in industry and by academic circuit design groups. Today the EKV v2.6 model is available with most of the major commercial simulators and a growing number of GPL simulators. The Verilog-A code for the Qucs ADMS\(^3\) compiled version of the EKV v2.6 model is given in an appendix to this report.

Effects modelled

The EKV v2.6 MOSFET model includes the following effects:

- Basic geometrical and process related features dependent on oxide thickness, junction depth, effective channel length and width
- Effects of doping profile
- Modelling of weak, moderate and strong inversion behaviour
- Modelling of mobility effects due to vertical and lateral fields, velocity saturation
- Short channel effects including channel-length modulation, source and drain charge-sharing and reverse channel effect
- Modelling of substrate current due to impact ionization
- Thermal and flicker noise
- First order non-quasistatic model for the transconductances

\(^1\)An example EDD macromodel of the short channel EKV 2.6 model can be found at [http://qucs.sourceforge.net/](http://qucs.sourceforge.net/).


\(^3\)Lemaitre L. and GU B., ADMS - a fully customizable Verilog-AMS compiler approach, MOS-AK Meeting, Montreux. Available from [http://www.mos-ak.org/montreux/posters/17_Lemaitre_MOS-AK06.pdf](http://www.mos-ak.org/montreux/posters/17_Lemaitre_MOS-AK06.pdf)
The Qucs implementation of the short channel EKV v2.6 model includes nearly all the features listed above. A simpler long channel version of the model is also available for those simulations that do not require short channel effects. Both nMOS and pMOS devices have been implemented. No attempt is made in this report to describe the physics of the EKV v2.6 model. Readers who are interested in learning more about the background to the model, its physics and function should consult the following references:


The Qucs long channel EKV v2.6 model

A basic DC model for the long channel nMOS EKV v2.6 model is given at the EKV Compact MOSFET model website. Unfortunately, this model is only of limited practical use due to its restricted modelling features. It does however, provide a very good introduction to compact device modelling using the Verilog-A hardware description language. Readers who are unfamiliar with the Verilog-A hardware description language should consult the following references:

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4This first release of the Qucs implementation of the EKV v2.6 MOSFET model does not include the first-order non-quasistatic model for transconductances.
6No dynamic, noise or temperature effects.
The equivalent circuit of the Qucs EKV long channel n type MOSFET model is shown in Fig. 1. In this model the inner section, enclosed with the red dotted box, represents the fundamental intrinsic EKV v2.6 elements. The remaining components model extrinsic elements which represent the physical components connecting the intrinsic MOSFET model to its external signal pins. In the Qucs implementation of the EKV v2.6 long channel MOSFET model the drain to source DC current \( I_{ds} \) is represented by the equations listed in a later section of the report, capacitors \( C_{gdi}, C_{gsi}, C_{dbi} \) and \( C_{sbi} \) are intrinsic components derived from the charge-based EKV equations, capacitors \( C_{gdo}, C_{gso} \) and \( C_{gbo} \) represent external overlap elements, the two diodes model the drain to channel and source to channel junctions (including diode capacitance) and resistors \( R_{Deff} \) and \( R_{Seff} \) model series connection resistors in the drain and source signal paths respectively.

**Long channel model parameters (LEVEL = 1)**

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### Fundamental long channel DC model equations (LEVEL = 1)

\[
\begin{align*}
V_g &= V(Gate) - V(Bulk) \\
V_s &= V(Source) - V(Bulk) \\
V_d &= V(Drain) - V(Bulk) \\
VGprime &= V_g - Vto + Phi + Gamma \cdot \sqrt{Phi} \\
V_p &= VGprime - Phi - Gamma \cdot \left( \sqrt{VGprime + \frac{\Gamma}{2}} \right)^2 - \frac{\Gamma}{2} \\
n &= 1 + \frac{\Gamma}{2 \cdot \sqrt{V_p + Phi + 4 \cdot Vt}} \\
\beta &= \frac{Kp}{W} \cdot \frac{1}{1 + Theta \cdot Vp} \\
X1 &= \frac{V_p - V_s}{Vt} \quad If = \left[ \ln \left\{ 1 + \lim\exp\left( \frac{X1}{2} \right) \right\} \right]^2 \\
X2 &= \frac{V_p - V_d}{Vt} \quad Ir = \left[ \ln \left\{ 1 + \lim\exp\left( \frac{X2}{2} \right) \right\} \right]^2 \\
I_{specific} &= 2 \cdot n \cdot \beta \cdot Vt^2
\end{align*}
\]
\[ Ids = Ispecific \cdot (If - Ir) \]

Where \( VG' \) is the effective gate voltage, \( Vp \) is the pinch-off voltage, \( n \) is the slope factor, \( \beta \) is a transconductance parameter, \( Ispecific \) is the specific current, \( If \) is the forward current, \( Ir \) is the reverse current, \( Vt \) is the thermal voltage at the device temperature, and \( Ids \) is the drain to source current. EKV v2.6 equation numbers are given in “< >” brackets at the left-hand side of each equation. Typical plots of Ids against Vds for both the nMOS and pMOS long channel devices are given in Figure 2.
Figure 2: Ids versus Vds plots for the Qucs EKV v2.6 long channel nMOS and pMOS models
**Testing model performance**

Implementing advanced component models like the EKV v2.6 MOSFET model is a complex process, involving the translation of a set of equations into the Verilog-A hardware design language, conversion of the Verilog-A code into C++ code via the ADMS compiler, and finally compiling and linking the model code with the main body of Qucs code. At all stages in the process accuracy becomes an important issue. This section of the Qucs EKV v2.6 report introduces a number of test simulations which were used during the model development cycle to check the performance of the Qucs EKV v2.6 implementation. The tests also demonstrate how a circuit simulator can be used to extract model parameters. The values of which help to confirm correct model operation.

**Extraction of Ispec**

When a MOS transistor is operating in the saturation region, reverse current \( I_r \) approaches zero and the drain to source current is approximated by

\[
I_{ds} = \text{Ispecific} \cdot f = \text{Ispecific} \cdot \left[ \ln\{1 + \text{limexp}\left(\frac{V_p - V_s}{2 \cdot V_t}\right)\} \right]^2
\]  

(1)

In saturation \( \text{limexp}\left(\frac{V_p - V_s}{2 \cdot V_t}\right) \gg 1 \), yielding

\[
\sqrt{I_{ds}} = \frac{\text{Ispecific}}{2 \cdot V_t^2} \cdot (V_p - V_s)
\]

(2)

Hence

\[
\frac{\partial(\sqrt{I_{ds}})}{\partial V_s} = \frac{\text{Ispecific}}{2 \cdot V_t^2} = -\text{slope}
\]

(3)

Or

\[
\text{Ispecific} = 2 \cdot \text{slope}^2 \cdot V_t^2
\]

(4)

Figure 3 shows a typical test circuit configuration for measuring and simulating \( I_{ds} \) with varying \( V_s \). Qucs post-simulation functions in equation block Eqn1 are used to calculate the value for \( \text{Ispecific} \). The value of \( \text{Ispecific} \) for the nMOS transistor with the parameters given in Fig. 3 is 3.95e-8 A. Figure 4 illustrates a test circuit for measuring \( V_p \) with the transistor in saturation. In this circuit \( I_s = \text{Ispecific} \) and the threshold voltage corresponds to \( V_q \) when \( V_p = 0 \). Notice also that \( n = \partial V_q/\partial V_p \). In Fig. 4 Qucs post-simulation processing functions are also used to generate data for \( V_p \), \( V_G' \) and \( n \). The value of the threshold voltage for the device shown in Fig. 4 is 0.6V. At this voltage \( n = 1.37 \). The two test configurations illustrated in Figs. 3 and 4 go some way to confirming that the Qucs implementation of the EKV v2.6 long channel model is functioning correctly.
Figure 3: Ispecific extraction test circuit and post simulation data processing results
Parameter sweep

SW1
Sim=DC1
Type=lin
Param=Vg
Start=0
Stop=1
Points=101

dc simulation

EKV26nMOS1
LEVEL=1
L=10e-6
W=10e-6
Cox=3.45e-3
Vto=0.6
Gamma=0.71
Phi=0.97

Equation

Eqn1
VGprime=Vg-Vto+Phi+Gamma*sqrt(Phi)
Gamma=0.71
Vto=0.6
Phi=0.97

Vp=VGprime-Phi-Gamma*(sqrt( VGprime+(Gamma/2)*(Gamma/2) ) -Gamma/2)
n=diff(Vg, Vs.V)

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<tr>
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<th>Vp</th>
<th>VGprime</th>
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<td>1.3658</td>
<td>0.0179</td>
<td>0.0147</td>
<td>1.69</td>
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</tbody>
</table>

Figure 4: Vp extraction test circuit and post simulation data processing results
Extraction of model intrinsic capacitance

The Qucs implementation of the EKV v2.6 MOSFET model uses the charge-based model for transcapacitances. This model ensures charge-conservation during transient analysis. Both the long channel and short channel versions employ the quasi-static charge-based model. The EKV v2.6 charge equations for the long channel intrinsic device are:

\[
q = 1 + \frac{\text{\( \text{Gamma} \)}}{2 \cdot \sqrt{Vp + Phi + 1e - 6}} \quad (5)
\]

\[
Xf = \sqrt{\frac{1}{4} + If} \quad (6)
\]

\[
Xr = \sqrt{\frac{1}{4} + Ir} \quad (7)
\]

\[
quid = -nq \cdot \left\{ \frac{4}{15} \cdot \frac{3 \cdot Xr^3 + 6 \cdot Xr^2 \cdot Xf + 4 \cdot Xr \cdot Xf^2 + 2 \cdot Xf^3}{(Xf + Xr)^2} - \frac{1}{2} \right\} \quad (8)
\]

\[
quis = -nq \cdot \left\{ \frac{4}{15} \cdot \frac{3 \cdot Xf^3 + 6 \cdot Xf^2 \cdot Xr + 4 \cdot Xf \cdot Xr^2 + 2 \cdot Xr^3}{(Xf + Xr)^2} - \frac{1}{2} \right\} \quad (9)
\]

\[
qu = quis + quid = -nq \cdot \left\{ \frac{4}{3} \cdot \frac{3 \cdot Xf^3 + Xr \cdot Xf + Xr^2}{Xf + Xr} - 1 \right\} \quad (10)
\]

\[
qub = -\text{\( \text{Gamma} \)} \cdot \sqrt{Vp + Phi + 1e - 6} \cdot \frac{1}{Vt} - \left( \frac{nq - 1}{nq} \right) \cdot qu \quad \forall (VGprime > 0) \quad (11)
\]

\[
qub = -VGprime \cdot \frac{1}{Vt} \quad \forall (VGprime \leq 0) \quad (12)
\]

\[
qug = -qu - qub \quad (13)
\]

\[
COX = Cox \cdot Np \cdot Weff \cdot Ns \cdot Leff \quad (14)
\]

\[
Q(I, B, D, S, G) = COX \cdot Vt \cdot q(I, B, D, S, G) \quad (15)
\]

The first release of the Qucs EKV v2.6 MOSFET model assumes that the gate and bulk charge is partitioned between the drain and source in equal ratio\(^7\). Fifty percent charge portioning yields the following \(Ids\) current contributions:

\[
I(Gate, Source\_int) < +0.5 \cdot p_{n\_MOS} \cdot ddt(QG) \quad (16)
\]

\(^7\)For an example of this type of charge partitioning see F. Pregaldiny et. al., An analytic quantum model for the surface potential of deep-submicron MOSFETS, 10th International Conference, MIXDES 2003, Lodz, Poland, 26-28 June 2003.
\[ I(Gate, Drain_{int}) < +0.5 \cdot p_{n\_MOS} \cdot ddt(QG) \]  
(17)

\[ I(Source_{int}, Bulk) < +0.5 \cdot p_{n\_MOS} \cdot ddt(QB) \]  
(18)

\[ I(drain_{int}, Bulk) < +0.5 \cdot p_{n\_MOS} \cdot ddt(QB) \]  
(19)

Where \( p_{n\_MOS} = 1 \) for nMOS devices or -1 for pMOS devices. Charge associated with the extrinsic overlap capacitors, \( C_{gs0}, C_{gd0} \) and \( C_{gb0} \), is represented in the Qucs EKV v2.6 implementation by the following equations:

\[ Q_{gs0} = C_{gs0} \cdot Weff \cdot Np \cdot (VG - VS) \]  
(20)

\[ Q_{gd0} = C_{gd0} \cdot Weff \cdot Np \cdot (VG - VD) \]  
(21)

\[ Q_{gb0} = C_{gb0} \cdot Leff \cdot Np \cdot VB \]  
(22)

The drain to bulk and source to bulk diodes also introduce additional components in the extrinsic capacitance model. The default value of \( C_{J0} \) being set at 300fF. Analysis of the y-parameters\(^8\) for the EKV v2.6 equivalent circuit shown in the test circuit illustrated in Fig. 5 yields

\[ y_{11} = \frac{j \cdot \omega \cdot C_g}{1 + \omega^2 \cdot (Rgn \cdot C_g)^2} \]  
(23)

Or

\[ y_{11} \cong \omega^2 \cdot Rg \cdot C_g^2 + j \cdot \omega \cdot C_g, \text{ when } \omega \cdot Rg \cdot C_g << 1. \]  
(24)

Hence, \( C_g = \text{imag}(y_{11}/\omega) \) and \( Rgn = \text{real}(y_{11}/(\omega^2 \cdot C_g^2)) \), where \( \omega = 2 \cdot \pi \cdot f \), and \( f \) is the frequency of y-parameter measurement, \( Rg \) is a series extrinsic gate resistance and \( C_g \approx C_{gs} + C_{gd} + C_{gb} \). With equal partitioning of the intrinsic gate charge \( C_gb \) approximates to zero and \( C_g \approx C_{gs} + C_{gd} \). The data illustrated in Figures 5 and 6 shows two features which are worth commenting on; firstly the values of \( C_g \) are very much in line with simple hand calculations (for example in the case of the nMOS device \( C_g(max) = W \cdot L \cdot Cox = 10e - 6 * 10e - 6 * 3.45e - 3 = 3.45e - 13F \)) and secondly both sets of simulation data indicate the correct values for the nMOS and pMOS threshold voltages (for example -0.55 V for the pMOS device and 0.6 V for the nMOS device), reinforcing confidence in the EKV v2.6 model implementation.

\(^8\)A more detailed analysis of the EKV v2.6 y-parameters can be found in F. Krummenacher et. al., HF MOSET MODEL parameter extraction, European Project No. 25710, Deliverable D2.3, July 28, 2000.
Figure 5: $y_{11}$ test circuit and values of $C_g$ for the long channel EKV v2.6 nMOS model
Figure 6: $y_{11}$ test circuit and values of Cg for the long channel EKV v2.6 pMOS model
Extraction of extrinsic diode capacitance and drain resistance

The extrinsic section of the EKV v2.6 model includes diodes which in turn are modelled by conventional DC characteristics and parallel capacitance. This capacitance is represented by depletion layer capacitance in the diode reverse bias region of operation. In the diode forward bias section of the I-V characteristic diffusion capacitance dominates. Figure 7 illustrates a test circuit that allows the diode capacitance to be extracted as a function of $V_{ds}$. In Fig. 7 the nMOS device is turned off and the drain to bulk diode reverse biased. Simple analysis indicates that

$$y_{11} \cong \omega^2 \cdot R_{Df} \cdot C_d^2 + j \cdot \omega \cdot C_d, \quad \text{when } \omega \cdot R_{Df} \cdot C_d << 1.$$  \hspace{1cm} (25)

Hence, $C_d = \text{imag}(y_{11}/\omega)$ and $R_{Df} = \text{real}(y_{11}/(\omega^2 \cdot C_d^2))$, where $\omega = 2 \cdot \pi \cdot f$, $f$ is the frequency of $y$-parameter measurement, and $C_d$ is the diode capacitance. The data shown in Fig. 7 indicate good agreement with the expected values for $C_d$ and $R_{Df}$; which are expected to be $C_d = 300\text{fF}$ at $V_{ds}=0V$, and $R_{Df} = 46\Omega$.

Simulating EKV v2.6 MOSFET noise

The EKV v2.6 intrinsic device noise is modelled by a noise current source connected between the internal drain and source terminals. The noise current source $I_{dsn}$, see Fig. 1, is composed of a thermal noise component and a flicker noise component. The Power Spectral Density ($S_{PSD}$) of these components are given by:

$$S_{PSD} = S_{\text{thermal}} + S_{\text{flicker}}$$  \hspace{1cm} (26)

Where

- Thermal noise
  $$S_{\text{thermal}} = 4 \cdot k \cdot T \cdot \beta \cdot |qI|$$  \hspace{1cm} (27)

- Flicker noise
  $$S_{\text{flicker}} = \frac{K \cdot g_{mg}^2}{N_p \cdot W_{eff} \cdot N_s \cdot L_{eff} \cdot C_{ox} \cdot f^A f},$$  \hspace{1cm} (28)

  $$g_{mg} = \frac{\partial I_{ds}}{\partial V_{gs}} = \beta \cdot V_t \cdot \left( \sqrt{\frac{4 \cdot I_f}{I_{specific}}} + 1 - \sqrt{\frac{4 \cdot I_r}{I_{specific}}} + 1 \right)$$  \hspace{1cm} (29)

Where $\beta$ is a transconductance factor, $qI = qD + qS$, and the other symbols are defined in the EKV v2.6 long channel parameter list or have their usual meaning. Noise has been implemented in both the Qucs long channel and short channel EKV v2.6 models. In addition to the intrinsic device noise the Qucs EKV v2.6 model includes the thermal noise components for both extrinsic resistors $R_{Df}$ and $R_{Seff}$. Figure 8 presents a typical noise test circuit and simulated noise currents. In Figure 8 four nMOS devices are biased under different DC conditions and their noise current simulated for a range of $W$ values.
Figure 7: Test circuit for extracting EKV v2.6 extrinsic diode capacitance
Figure 8: Test circuit for simulating EKV v2.6 noise: Ids in blue curve, Ids1 in red curve, Ids2 in black curve and Ids3 in green curve

between 1e-6 m and 100e-6 m. The first three devices include both thermal and flicker noise components ($KF = 1e-27$) while the fourth device has its flicker component set to zero. The resulting current noise curves clearly demonstrate the effect of summing intrinsic thermal and flicker components on the overall performance of the EKV v2.6 noise model.

The Qucs short channel EKV v2.6 model

The Qucs implementation of the short short channel EKV v2.6 MOSFET model contains all the features implemented in the long channel version of the model plus a number of characteristics specific to short channel operation. However, the short channel version of the model does not use parameter Theta. Parameter LEVEL set to 2 selects the short channel model. Both pMOS and nMOS versions of the model are available for both long and short channel implementations. The entire short channel EKV v2.6 MOSFET model
is described by roughly 94 equations. Readers who are interested in the mathematics of the model should consult “The EPFL-EKV MOSFET Model Equations for Simulation” publication cited in previous text. Appendix A lists the complete Verilog-A code for the first release of the Qucs EKV v2.6 MOSFET models. Additional Verilog-A code has been added to the model equation code to (1) allow interchange of the drain and source terminals, and (2) select nMOS or pMOS devices.

**Short channel model parameters (LEVEL = 2)**

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17
Simulating short channel charge sharing effects

A simple test circuit for demonstrating the effects of charge sharing is given in Figure 9. With charge sharing disabled, by setting \( W_{\text{eta}} \) and \( L_{\text{eta}} \) to zero, the magnitude and slope of the \( I_d \) vs. \( V_{ds} \) curve shows a marked difference to that where charge sharing is enabled. One point to note with this test: charge sharing in short channel devices significantly reduces the device output resistance which could have, of course, important consequences on circuit performance.

End note

This report outlines some of the background to the Qucs implementation of the EKV v2.6 MOSFET model. A series of test results demonstrate a range of results that have been
achieved with this new Qucs compact device model. Although the test results give data similar to what is expected in all cases it must be stressed that this is the first release of this MOSFET model and as such it will probably contain bugs. A great deal of work has gone into providing this new Qucs model. However, all the effort has been worthwhile because for the first time Qucs now has a submicron MOSFET model. Please use the model and report bugs to the Qucs development team. Much work still remains to be done in the development of MOSFET models for Qucs. In future releases both bug fixes and new models are likely to feature strongly. Once again I would like to thank Stefan Jahn and Władysław Grabiński (of MOS-AK) for their encouragement and support during the period I have been working on developing the Qucs implementation of the EKV v2.6 model and writing this report.

Qucs Verilog-A code for the EKV v2.6 MOSFET model

nMOS: EKV equation numbers are given on the right-hand side of code lines

```verilog
// Qucs EPFL EKV 2.6 nMOS model:
//
// The structure and theoretical background to the EKV 2.6
// Verilog-a model is presented in the Qucs EPFL EKV 2.6 report.
// Typical parameters are for 0.5um CMOS (C) EPFL-LEG 1999.
// Geometry range: Short channel W >= 0.8um, L >= 0.5um
// Long channel W >= 2um, L >= 2um
// Voltage range: |Vgb| < 3.3V, |Vdb| < 3.3V, |Vsb| < 2V
//
// This is free software; you can redistribute it and/or modify
// it under the terms of the GNU General Public License as published by
// the Free Software Foundation; either version 2, or (at your option)
// any later version.
//
// Copyright (C), Mike Brinson, mbrin72043@yahoo.co.uk, May 2008.
//
// `include "disciplines.vams"
// `include "constants.vams"

module EKV26nMOS (Drain, Gate, Source, Bulk);
    inout Drain, Gate, Source, Bulk;
    electrical Drain, Gate, Source, Bulk;
// Internal nodes
electrical Drain_int, Source_int;
define attr(txt) (*txt*)
// Device dimension parameters
parameter real LEVEL = 1 from [1 : 2]
    `attr(info="long_{1}, short_{2}");
parameter real L = 0.5e-6 from [0.0 : inf]
    `attr(info="length_{parameter}" unit = "m");
parameter real W = 10e-6 from [0.0 : inf]
    `attr(info="Width_{parameter}" unit = "m");
parameter real Np = 1.0 from [1.0 : inf]
    `attr(info="parallel_{multiple_device_number}");
parameter real Ns = 1.0 from [1.0 : inf]
    `attr(info="series_{multiple_device_number}"");
// Process parameters
```
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Range</th>
<th>Units</th>
</tr>
</thead>
<tbody>
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parameter real Ibn = 1.0 from [0.1 : inf]
  "attr(info="saturation_currentsaturation_voltage_factor") for
  impact ionization");
// Flicker noise parameters
parameter real Kf = 1.0e-27 from [0.0 : inf]
  "attr(info="flicker_noise_flicker_noise_coefficient")
parameter real Af = 1.0 from [0.0 : inf]
  "attr(info="flicker_noise_flicker_noise_exponent")
// Matching parameters
parameter real Avto = 0.0 from [0.0 : inf]
  "attr(info="area_related_threshold_voltage_mismatch_parameter") unit = "V*m"
parameter real Akp = 0.0 from [0.0 : inf]
  "attr(info="area_related_gain_mismatch_parameter") unit="m"
parameter real Agamma = 0.0 from [0.0 : inf]
  "attr(info="area_related_body_effect_mismatch_parameter") unit=sqrt(V)*m"
// Diode parameters
parameter real N=1.0 from [1e-6: inf]
  "attr(info="emission_coefficient")
parameter real Is=1e-14 from [1e-20: inf]
  "attr(info="saturation_current saturaton_current") unit="A"
parameter real Bv=100 from [1e-6: inf]
  "attr(info="reverse_breakdown_voltage") unit="V"
parameter real Vj=1.0 from [1e-6: inf]
  "attr(info="junction_potential") unit="V"
parameter real Cj0=300e-15 from [0: inf]
  "attr(info="zero_bias_junction_capacitance") unit="F"
parameter real M=0.5 from [1e-6: inf]
  "attr(info="grading_coefficient")
parameter real Area=1.0 from [1e-3: inf]
  "attr(info="diode_relative_area")
parameter real Fc=0.5 from [1e-6: inf]
  "attr(info="forward_bias_depletion_capcitance_coefficient")
parameter real Tt=0.1e-9 from [1e-20: inf]
  "attr(info="transit_time") unit="s"
parameter real Xti=3.0 from [1e-6: inf]
  "attr(info="saturation_current_temperature_exponent")
// Temperature parameters
parameter real Thom = 26.85
  "attr(info="parameter_measurement_temperature") unit = "Celsius"
// Local variables
real epsilon_s, epsilon_o, Tnom, T2, Tratio, Vto_T, Ucrit_T, Eg0nom, Ed, Phi_T;
real Weff, Leff, RDeff, RSeff, con1, con2, Vto, Kp, Kpa_T, Gamma, C epsilon, xi;
real nn, deltaV_RSC, Vg, Vs, Vd, Vgs, Vgd, Vds, Vds0, VG, VS, VD;
real VGprime, VP0, VSp, VDprime, Gamma0, Gammaprime, Vp;
real n, X1, iff, X2, ir, Vc, Vds, Vdssprime, deltaV, Vf;
real Lc, DeltaL, Lprime, Lmin, X3, irprime, Beta0, eta;
real Qb0, Beta0prime, qg0, X, Kr, qP, qL, qB, Beta, Ispecific, Ids, Vb, Idb, Ibb_T;
real A, B, Vt, T2, E_T1, E_T2, V_T2, C0_T2, F1, F2, F3, I_T2;
real Id1, Id2, Id3, Id4, Is1, Is2, Is3, Is4, V1, V2, Ib_d, Ib_s, Qd, Qs, Qd_T, Qs_T, Qd1, Qs1, Qd2, Qs2;
real qB, qg0, qg0, qg0, fourk, Sthermal, gm, Sflicker, StoSwap, p_mOS;
// analog begin
   // Equation initialization
p_mOS = 1.0; // nMOS
A=7.02e-4;
B=1108.0;
epsilon_s = 1.0359e-10; // Eqn 4
epsilon_o = 3.453143e-11; // Eqn 5
Tnom = Thon+273.15; // Eqn 6
T2=Temperature;
Tratio = T2/Tnom;
Vto_T = Vto-Tcv*(T2-Tnom);
Eg0nom = 1.16-0.000702*Tnom+0.000702*(Tnom+1108);
Eg = 1.16-0.000702*T2+(T2+1108):
\[ \Phi_T = \Phi \times \text{Tratio} - 3.0 \times \$vt \times \ln(\text{Tratio}) - \text{Egnom} \times \text{Tratio} + \text{Eg}; \]

\[ I_{bb_T} = I_{bb} \times (1.0 + I_{bb} \times (T_2 - T_{nomk})); \]

\[ \text{Weff} = W + Dc; \quad \text{Eqn 25} \]

\[ \text{Leff} = L + Dl; \quad \text{Eqn 26} \]

\[ \text{RDeff} = \left( \frac{H_{dif} \times \text{Rsh}}{\text{Weff}} \right) / N_p + \text{Rdc}; \]

\[ \text{RSeff} = \left( \frac{H_{dif} \times \text{Rsh}}{\text{Weff}} \right) / N_p + \text{Rsc}; \]

\[ \text{con1} = \sqrt{N_p \times \text{Weff} \times N_s \times \text{Leff}}; \]

\[ V_{t_{T2}} = P_{K} \times \sqrt[4]{T_2}; \quad \text{Eqn 27} \]

\[ K_{pa} = K_p \times (1.0 + \text{Apk} / \text{con1}); \quad \text{Eqn 28} \]

\[ K_{pa_T} = K_{pa} \times \text{pow}(\text{Tratio}, B_{ex}); \quad \text{Eqn 18} \]

\[ \text{Gammaa} = \text{Gamma} + \text{Agamma} / \text{con1}; \quad \text{Eqn 29} \]

\[ \text{Cepsilon} = 4.0 \times \text{pow}(22 \times e - 3, 2); \quad \text{Eqn 30} \]

\[ \text{xi} = 0.028 \times (10.0 \times (\text{Leff} / L_k) - 1.0); \quad \text{Eqn 31} \]

\[ \text{nnn} = 1.0 + 0.5 \times (\text{xi} + \sqrt{\text{pow}(\text{xi}^2 + C_{epsilon})}); \]

\[ \delta V_{RSCE} = (2.0 \times Q_0 / \text{Cox}) \times (1.0 / \text{pow}(\text{nnn}, 2)); \quad \text{Eqn 32} \]

\[ \text{Vg} = \text{p-n MOS} \times V(\text{Gate}, \text{Bulk}); \]

\[ \text{Vs} = \text{p-n MOS} \times V(\text{Source}, \text{Bulk}); \]

\[ \text{Vd} = \text{p-n MOS} \times V(\text{Drain}, \text{Bulk}); \]

\[ \text{VG} = \text{Vg}; \quad \text{Eqn 22} \]

\[ \text{if} \quad ((\text{Vd} - \text{Vs}) \geq 0.0) \]

\[ \begin{align*}
\text{StoDswap} &= 1.0; \\
\text{VS} &= \text{Vs}; \quad \text{Eqn 23} \\
\text{VD} &= \text{Vd}; \quad \text{Eqn 24}
\end{align*} \]

\[ \text{if} \quad (\text{LEVEL} == 2) \]

\[ \text{VGprime} = \text{VG} - \Phi_T - \text{Gammaa} \times \sqrt{\text{VGprime} + \text{Gammaa} / 2.0}; \quad \text{Eqn 33} \]

\[ \text{if} \quad (\text{LEVEL} == 2) \]

\[ \text{VGprime} = \text{VG} - \Phi_T + \text{Gammaa} \times \sqrt{\text{VGprime} + \text{Gammaa} / 2.0}; \quad \text{Eqn 33} \]

\[ \text{if} \quad (\text{VGprime} > 0) \]

\[ \begin{align*}
\text{VP0} &= \text{VGprime} - \text{Gammaa} \times (\sqrt{\text{VGprime} + \text{Gammaa} / 2.0}); \quad \text{Eqn 34} \\
\text{VP} &= \text{VP0}; \\
\text{Vprime} &= 0.5 \times (\text{VS} + \Phi_T + \sqrt{\text{pow}((\text{VS} + \Phi_T, 2) + \text{pow}((4.0 \times \$vt, 2))}); \quad \text{Eqn 35}
\end{align*} \]
\[
\begin{align*}
VD&=0.5*(V_{D}+\Phi_I+T)+\text{sqrt}(pow(V_{D}+\Phi_I+T,2)+pow(4.0*$vt,2)); \quad // Eqn 35 \\
\text{Gamma}0&=\text{Gamma}0-(\text{epsilon}_0/C_{ox})*\left((\text{Len}+\text{Leff})\text{sqrt}(V_{prime}+\text{sqrt}(\text{VD}))-\text{sqrt}(V_{prime}+\text{sqrt}(\text{Vprime}+\text{Gamma}/2.0))\right); \quad // Eqn 36 \\
\text{Gamma}prime&=0.5*(\text{Gamma}0\text{sqrt}(pow(\text{Gamma}0,2)+0.1*$vt)); \quad // Eqn 37 \\
\text{if} (V_{prime}>0.0) & \quad V_P=V_{prime}-\Phi_I-\text{Gamma}prime*(\text{sqrt}(V_{prime}+(\text{Gamma}prime/2.0))*(\text{Gamma}prime/2.0))-\text{Gamma}prime/2.0)); \quad // Eqn 38 \\
\text{else} & \quad V_P=-\Phi_I; \\
n&=1.0+\text{Gamma}0/(2.0*\text{sqrt}(V_P+\Phi_I+4.0*$vt)); \quad // Eqn 39 \\
\text{endif} \\
\text{begin} & \quad \text{if} (\text{Vprime}<0.0) & \quad V_P=V_{prime}-\Phi_I-\text{Gamma}prime*(\text{sqrt}(V_{prime}+(\text{Gamma}prime/2.0))*(\text{Gamma}prime/2.0)); \quad // Eqn 34 \\
\text{else} & \quad V_P=-\Phi_I; \\
n&=1.0+\text{Gamma}0/(2.0*\text{sqrt}(V_P+\Phi_I+4.0*$vt)); \quad // Eqn 39 \\
\text{endif} \\
\text{begin} & \quad \text{if} (\text{LEVEL}==2) & \quad \text{begin} \\
Vc &= \text{Ucrit}*\text{N}_s*\text{Leff}; \quad // Eqn 45 \\
Vdss &= Vc*(sqrt(0.25+((\text{sqrt}Vc/\text{Vc}))*\text{sqrt}(\text{iff}))-0.5); \quad // Eqn 46; \\
\text{Vdssprime} &= Vc*(sqrt(0.25+((\text{sqrt}Vc/\text{Vc}))*\text{sqrt}(\text{iff}))-0.5)*\text{sqrt}((\text{Vc}/(2.0*$vt))-0.6); \quad // Eqn 47 \\
\text{if} (\text{Lambda}*(\text{sqrt}(\text{iff}))>(\text{Vdss}/\text{Vc})) & \quad \delta \text{V} = \text{sqrt}(\delta \text{V}^2+\text{pow}(\text{deltaV},2)); \quad // Eqn 48 \\
\text{else} & \quad \text{deltaV} = 1.0/64.0; \quad // Eqn 48 \\
\text{endif} \\
Vdso &= (\text{Vc}+\text{Phi}_0)/2.0; \quad // Eqn 49 \\
\text{Vip} &= \text{sqrt}((\text{pow}Vdd_2,2)+\text{pow}(\text{deltaV}_2,2))-\text{sqrt}((\text{pow}Vdd_2,2)+\text{pow}(\text{deltaV}_2,2)); \quad // Eqn 49; \\
Lc &= \text{sqrt}((\epsilon_0/C_{ox})*X_j); \quad // Eqn 51 \\
\text{DeltaL} &= \text{Lambda}+\text{Leff}/10.0; \quad // Eqn 54 \\
\text{leq} &= (\text{Leq}*(\text{sqrt}(\text{pow}(\text{Lprime},2)+\text{pow}(\text{Leff},2)))); \quad // Eqn 55; \\
X3 &= (\text{sqrt}(\text{pow}(\text{Vdss}_2,2)+\text{pow}(\text{deltaV}_2,2))+\text{sqrt}(\text{pow}(\text{Vdso}+\text{Vip}),2)+\text{sqrt}(\text{pow}(\text{Vdssprime}),2)+\text{sqrt}(\text{pow}Vddprime,2))/\text{sqrt}((\text{pow}Vddprime,2))/\text{sqrt}((\text{.IsNotNullC})); \quad // Eqn 56; \\
\text{Beta0} &= \text{Kpa}_T*(\text{nMOS}+\text{Leff}+\text{Vc}/\text{Leff}); \quad // Eqn 57 \\
\text{eta} &= 0.5; \quad // Eqn 59; \\
\text{Beta0prime} &= \text{Beta0}*(\text{1.0}+\text{Cox}/(\text{EO}+\epsilon_0)); \quad // Eqn 60; \\
nq &= 1.0+\text{Gamma}0/(2.0*\text{sqrt}(V_P+\Phi_I+\text{leq}-6)); \quad // Eqn 61 \\
\text{endif} \\
\text{begin} & \quad \text{if} (\text{LEVEL}==2) & \quad \text{begin} \\
Xf &= \text{sqrt}(0.25+\text{iff}); \quad // Eqn 70 \\
\text{Xr} &= \text{sqrt}(0.25+\text{ir}); \quad // Eqn 71 \\
\text{qD} &= \text{qD}*(4.0/15.0)+\text{pow}(X_3,3)+6.0\times\text{pow}(X_2,2)\times\text{Xf}+4.0\times\text{Xf}\times\text{pow}(X,2) \quad \text{+} 2.0\times\text{pow}(\text{Xf},3))//\text{pow}(\text{Xf},2,2)) \quad -0.5; \quad // Eqn 72 \\
\text{qS} &= \text{qS}*(4.0/15.0)+\text{pow}(X_3,3)+6.0\times\text{pow}(X_2,2)\times\text{Xf}+4.0\times\text{Xf}\times\text{pow}(X_2,2) \quad \text{+} 2.0\times\text{pow}(\text{Xf},3))//\text{pow}(\text{Xf},2,2)) \quad -0.5; \quad // Eqn 73 \\
\text{ql} &= \text{ql}*(4.0/3.0)\times(\text{pow}(\text{Xf},2)+(\text{Xf}\times\text{Xr})+\text{pow}(\text{Xr},2))/(\text{Xf}\times\text{Xr}) \quad -1.0; \quad // Eqn 74 \\
\text{if} (\text{LEVEL}==2) & \quad \text{end} \\
\end{align*}
\]
if (VGprime > 0)
    qB = (-Gamma*$v*)*(1.0/$vt) - (nq-1.0)/nq)*qI;  // Eqn 75
else
    qB = -VGprime/$vt;

if (VGprime > 0)
    qB = (-Gamma*$v*)*(1.0/$vt) - (nq-1.0)/nq)*qI;  // Eqn 75
else
    qB = -VGprime/$vt;

if (LEVEL == 2)
    Beta = Beta0prime / (1.0 + (Cos/ (EO*epsilon_si)))*$vt*abs(qB+eta*qI));  // Eqn 62
else
    Beta = Kp*(Weff/Leff)/(1+Theta*VP);

Ispecific = 2.0*n*Beta*pow($vt, 2);  // Eqn 65

if (LEVEL == 2)
begin
    // Eqn 66
    Vib = VD-VDx-Ibn*2.0*Vds;
if (vib > 0.0)
    Idb = Ispecific*(1/2/2)*Vib*exp((-Ibb*T/Leff)/Vib);
end
else
    Idb = 0.0;
end

Ids = Ispecific*(1/2/2);
// Eqn 66
Thermal = fourkt*Beta*abs(qI);
gm = Beta*vt*(sqrt((4.0*If/Ispecific) + 1.0) - sqrt((4.0*ir/Ispecific) + 1.0));
Sflicker = (Kf*gm)/((Np*Weff*Ns*Leff*Cox);

// Drai and source diodes
if (StoDawap > 0.0)
begin
    V1=p_n_MOSxV(Bulk, Drain_int);
    V2=p_n_MOSxV(Bulk, Source_int);
end

Id1 = (V1-5.0*$vt) ? Area*Is_T2*(limexp(V1/(N*Vt*T2) -1.0) : 0;
Qd1 = (V1<Fc*Vj)? Ts+Id1*Area*(Cj0*T2*Vj*T2/(1-M))*(1-pow((1-V1/Vj*T2),(1-M))) : 0;
Id2 = (V1<5.0*$vt) ? Area*Is_T2 : 0;
Qd2 = (V1>Fc*Vj)? Ts*Id1*Area*(Cj0*T2*(F1+(1/F2))*(F3*(V1-Fc*Vj*T2)+M/(2.0*Vj*T2)) : 0;
Id3 = (V1 == -Bv) ? -Ivb : 0;
Id4 = (V1<0.0) ? Area*Is_T2*(limexp(-(Bv+V1)/Vt*T2) -1.0+Bv/Vt*T2) : 0;
Ib_d = Id1+Id2+Id3+Id4;
Qd = Qd1+Qd2;

// Is1 = (V2<5.0*$vt) ? Area*Is_T2*(limexp(V2/(N*Vt*T2) -1.0)) : 0;
Qs1 = (V2<Fc*Vj)? Ts*Is1*Area*(Cj0*T2*Vj*T2/(1-M))*(1-pow((1-V2/Vj*T2),(1-M))) : 0;
Is2 = (V2<5.0*$vt) ? Area*Is_T2 : 0;
Qs2 = (V2>Fc*Vj)? Ts*Is1*Area*(Cj0*T2*(F1+(1/F2))*(F3*(V2-Fc*Vj*T2)+M/(2.0*Vj*T2)) : 0;
Is3 = (V2 == -Bv) ? -Ivb : 0;
\[ I_{s4} = (V_2 - Bv) \cdot \text{Area} \cdot \frac{V_{2T2} + (Bv + V2)}{V_{T2}} - 1.0 = Bv/V_{T2} \cdot 0; \]

\[ I_{b,s} = I_{s1} + I_{s2} + I_{s3} + I_{s4}; \]

\[ Q_s = Q_{s1} + Q_{s2}; \]

/ Current and noise contributions

if (StoDswap > 0.0)

begin

if (RDeff > 0.0)

\[ I(\text{Drain}, \text{Drain\_int}) < V(\text{Drain}, \text{Drain\_int})/\text{RDeff}; \]

else

\[ I(\text{Drain}, \text{Drain\_int}) < V(\text{Drain}, \text{Drain\_int})/1e^{-7}; \]

if (RS eff > 0.0)

\[ I(\text{Source}, \text{Source\_int}) < V(\text{Source}, \text{Source\_int})/\text{RS eff}; \]

else

\[ I(\text{Source}, \text{Source\_int}) < V(\text{Source}, \text{Source\_int})/1e^{-7}; \]

\[ I(\text{Drain\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot I_{ds}; \]

if (LEVEL == 2)

\[ I(\text{Drain\_int}, \text{Bulk}) < p_{\text{nMOS}} \cdot I_{db}; \]

\[ I(\text{Gate}, \text{Drain\_int}) < p_{\text{nMOS}} \cdot 0.5 \cdot ddt(\text{qg}); \]

\[ I(\text{Gate}, \text{Source\_int}) < p_{\text{nMOS}} \cdot 0.5 \cdot ddt(\text{qg}); \]

\[ I(\text{Drain\_int}, \text{Bulk}) < p_{\text{nMOS}} \cdot 0.5 \cdot ddt(\text{qb}); \]

\[ I(\text{Source\_int}, \text{Bulk}) < p_{\text{nMOS}} \cdot 0.5 \cdot ddt(\text{qb}); \]

\[ I(\text{Gate}, \text{Drain\_int}) < p_{\text{nMOS}} \cdot ddt(\text{qgso}); \]

\[ I(\text{Gate}, \text{Drain\_int}) < p_{\text{nMOS}} \cdot \text{Ids}; \]

if (LEVEL == 2)

\[ I(\text{Gate\_int}, \text{Bulk}) < p_{\text{nMOS}} \cdot I_{db}; \]

\[ I(\text{Gate}, \text{Source\_int}) < p_{\text{nMOS}} \cdot 0.5 \cdot ddt(\text{qg}); \]

\[ I(\text{Gate\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot 0.5 \cdot ddt(\text{qg}); \]

\[ I(\text{Source\_int}, \text{Bulk}) < p_{\text{nMOS}} \cdot 0.5 \cdot ddt(\text{qb}); \]

\[ I(\text{Gate\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot ddt(\text{qgso}); \]

\[ I(\text{Gate\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot ddt(\text{qgdo}); \]

\[ I(\text{Gate}, \text{Bulk}) < p_{\text{nMOS}} \cdot ddt(\text{qgdo}); \]

\[ I(\text{Bulk}, \text{Drain\_int}) < p_{\text{nMOS}} \cdot I_{b,d}; \]

\[ I(\text{Bulk}, \text{Drain\_int}) < p_{\text{nMOS}} \cdot ddt(\text{Qd}); \]

\[ I(\text{Bulk}, \text{Source\_int}) < p_{\text{nMOS}} \cdot I_{bs}; \]

\[ I(\text{Bulk}, \text{Source\_int}) < p_{\text{nMOS}} \cdot ddt(\text{Qs}); \]

\[ I(\text{Drain\_int}, \text{Source\_int}) < \text{white\_noise}(\text{Sthermal},\"\text{thermal}\"); \]

\[ I(\text{Drain\_int}, \text{Source\_int}) < \text{flicker\_noise}(\text{Sflicker}, \text{Af}, \"\text{flicker}\""); \]

\[ I(\text{Drain\_int}, \text{Source\_int}) < \text{white\_noise}(\text{fourkt}/\text{RDeff}, \"\text{thermal}\"); \]

\[ I(\text{Source\_int}, \text{Source\_int}) < \text{white\_noise}(\text{fourkt}/\text{RS eff}, \"\text{thermal}\"); \]

end

else

begin

if (RS eff > 0.0)

\[ I(\text{Drain\_int}, \text{Drain\_int}) < V(\text{Drain}, \text{Drain\_int})/\text{RS eff}; \]

else

\[ I(\text{Drain\_int}, \text{Drain\_int}) < V(\text{Drain}, \text{Drain\_int})/1e^{-7}; \]

if (RDeff > 0.0)

\[ I(\text{Source}, \text{Source\_int}) < V(\text{Source}, \text{Source\_int})/\text{RDeff}; \]

else

\[ I(\text{Source}, \text{Source\_int}) < V(\text{Source}, \text{Source\_int})/1e^{-7}; \]

\[ I(\text{Source\_int}, \text{Drain\_int}) < p_{\text{nMOS}} \cdot I_{ds}; \]

if (LEVEL == 2)

\[ I(\text{Source\_int}, \text{Bulk}) < p_{\text{nMOS}} \cdot I_{db}; \]

\[ I(\text{Gate}, \text{Source\_int}) < p_{\text{nMOS}} \cdot 0.5 \cdot ddt(\text{qg}); \]

\[ I(\text{Gate\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot 0.5 \cdot ddt(\text{qg}); \]

\[ I(\text{Source\_int}, \text{Bulk}) < p_{\text{nMOS}} \cdot 0.5 \cdot ddt(\text{qb}); \]

\[ I(\text{Gate\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot ddt(\text{qgso}); \]

\[ I(\text{Gate\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot ddt(\text{qgdo}); \]

\[ I(\text{Gate}, \text{Bulk}) < p_{\text{nMOS}} \cdot ddt(\text{qgdo}); \]

\[ I(\text{Bulk\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot I_{bs}; \]

\[ I(\text{Bulk\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot ddt(\text{Qd}); \]

\[ I(\text{Bulk\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot I_{b,d}; \]

\[ I(\text{Bulk\_int}, \text{Source\_int}) < p_{\text{nMOS}} \cdot ddt(\text{Qs}); \]

\[ I(\text{Source\_int}, \text{Source\_int}) < \text{white\_noise}(\text{Sthermal},\"\text{thermal}\"); \]

\[ I(\text{Source\_int}, \text{Source\_int}) < \text{flicker\_noise}(\text{Sflicker}, \text{Af}, \"\text{flicker}\""); \]

\[ I(\text{Source\_int}, \text{Source\_int}) < \text{white\_noise}(\text{fourkt}/\text{RDeff}, \"\text{thermal}\"); \]

\[ I(\text{Source\_int}, \text{Source\_int}) < \text{white\_noise}(\text{fourkt}/\text{RS eff}, \"\text{thermal}\"); \]

end

end

endmodule
pMOS: EKV equation numbers are given on the right-hand side of code lines

// Qucs EPFL-EKV 2.6 pMOS model:

// The structure and theoretical background to the EKV 2.6
// Verilog-a model is presented in the Qucs EPL-EKV 2.6 report.
// Typical parameters are for 0.5um CMOS (C) EPLFL-LEG 1999.
// Geometry range: Short channel: W >= 0.8um, L >= 0.5um
// Long channel: W >= 2um, L >= 2um
// Voltage range: |Vgs| < 3.3V, |Vds| < 3.3V, |Vsb| < 2V

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// it under the terms of the GNU General Public License as published by
// the Free Software Foundation; either version 2, or (at your option)
// any later version.

// Copyright (C), Mike Brinson, mbrin72043@yahoo.co.uk, May 2008.

'include "disciplines.vams"
'include "constants.vams"

module EKV26pMOS (Drain, Gate, Source, Bulk);

// Internal nodes
electrical Drain_int, Source_int;
'define attr(txt) (*txt*)
// Device dimension parameters
parameter real LEVEL = 1 from [1 : 2]
  "attr(info="long\textsuperscript{2l},short\textsuperscript{22})");
parameter real L = 0.5e-6 from [0.0 : inf]
  "attr(info="length\_parameter" unit = "m")
parameter real W = 10e-6 from [0.0 : inf]
  "attr(info="Width\_parameter" unit = "m")
parameter real Np = 1.0 from [1.0 : inf]
  "attr(info="parallel\_multiple\_device\_number")
parameter real Ns = 1.0 from [1.0 : inf]
  "attr(info="series\_multiple\_device\_number")
// Process parameters
parameter real Cox = 3.45e-3 from [0 : inf]
  "attr(info="gate\_oxide\_capacitance\_per\_unit\_area" unit = "F/m\textsuperscript{2}")
parameter real Xj = 0.15e-6 from [0.0e-6 : 1.0e-6]
  "attr(info="metallurgical\_junction\_depth" unit = "m")
parameter real Dw = -0.05e-6 from [-inf : 0.0]
  "attr(info="channel\_width\_correction" unit = "m")
parameter real DI = -0.05e-6 from [-inf : 0.0]
  "attr(info="channel\_length\_correction" unit = "m")
// Basic intrinsic model parameters
parameter real Vto = -0.55 from [-inf : -1e-6]
  "attr(info="long\_channel\_threshold\_voltage" unit="V")
parameter real Gamma = 0.69 from [0.0 : 2.0]
  "attr(info="body\_effect\_parameter" unit="\textsuperscript{1/2}V")
parameter real Phi = 0.87 from [0.3 : 2.0]
  "attr(info="bulk\_Fermi\_potential" unit="V")
parameter real Kp = 35e-6 from [10e-6 : inf]
  "attr(info="transconductance\_parameter" unit = "A/V\textsuperscript{2}")
parameter real Theta = 50e-3 from [0.0 : inf]
  "attr(info="mobility\_reduction\_coefficient" unit = "1/V")
parameter real EO = 51.0e6 from [1.0e6 : inf]
  "attr(info="mobility\_coefficient" unit="V/m")
parameter real Ucrit = 18.0e6 from [2.0e6 : 25.0e6]
// Channel length and charge sharing parameters
parameter real Lambda = 1.1 from [0.1 : inf]
  'attr(info="longitudinal\_critical\_field") unit="V/m"
';
parameter real Weta = 0.0 from [0.0 : inf]
  'attr(info="depletion\_length\_coefficient")
';
parameter real Leta = 0.45 from [0.0 : inf]
  'attr(info="longitudinal\_critical\_field")
';
// Reverse short channel effect parameters
parameter real Q0 = 200e-6 from [0.0 : inf]
  'attr(info="reverse\_short\_channel\_charge\_density") unit="A*s/m^2"
';
parameter real Lk = 0.6e-6 from [0.0 : inf]
  'attr(info="characteristic\_length") unit="m"
';
// Intrinsic model temperature parameters
parameter real Tcv = -1.4e-3
  'attr(info="threshold\_voltage\_temperature\_coefficient") unit="V/K"
';
parameter real Bex = -1.4
  'attr(info="mobility\_temperature\_coefficient")
';
parameter real Ucex = 2.0
  'attr(info="Longitudinal\_critical\_field\_temperature\_exponent")
';
parameter real Ibbt = 0.0
  'attr(info="Ibb\_temperature\_coefficient") unit="1/K"
';
// Series resistance calculation parameters
parameter real Hdif = 0.9e-6 from [0.0 : inf]
  'attr(info="heavily\_doped\_diffusion\_length") unit="m"
';
parameter real Rsh = 990.0 from [0.0 : inf]
  'attr(info="drain\_source\_diffusion\_sheet\_resistance") unit="Ohm/square"
';
parameter real Rsc = 0.0 from [0.0 : inf]
  'attr(info="source\_contact\_resistance") unit="Ohm"
';
parameter real Rdc = 0.0 from [0.0 : inf]
  'attr(info="drain\_contact\_resistance") unit="Ohm"
';
// Gate overlap capacitances
parameter real Cgso = 1.5e-10 from [0.0 : inf]
  'attr(info="gate\_to\_source\_overlap\_capacitance") unit="F/m"
';
parameter real Cgdo = 1.5e-10 from [0.0 : inf]
  'attr(info="gate\_to\_drain\_overlap\_capacitance") unit="F/m"
';
parameter real Cgbo = 4.0e-10 from [0.0 : inf]
  'attr(info="gate\_to\_bulk\_overlap\_capacitance") unit="F/m"
';
// Impact ionization related parameters
parameter real Iba = 0.0 from [0.0 : inf]
  'attr(info="first\_impact\_ionization\_coefficient") unit="1/m"
';
parameter real Ibb = 3.0e8 from [1.0e8 : inf]
  'attr(info="second\_impact\_ionization\_coefficient") unit="V/m"
';
parameter real Ibn = 1.0 from [0.1 : inf]
  'attr(info="saturation\_voltage\_factor\_for\_impact\_ionization")
';
// Flicker noise parameters
parameter real Kf = 1.0e-28 from [0.0 : inf]
  'attr(info="flicker\_noise\_coefficient")
';
parameter real Af = 1.0 from [0.0 : inf]
  'attr(info="flicker\_noise\_exponent")
';
// Matching parameters
parameter real Avto = 0.0 from [0.0 : inf]
  'attr(info="area\_related\_threshold\_voltage\_mismatch\_parameter") unit="V*m"
';
parameter real Akp = 0.0 from [0.0 : inf]
  'attr(info="area\_related\_gain\_mismatch\_parameter") unit="m"
';
parameter real Agamma = 0.0 from [0.0 : inf]
  'attr(info="area\_related\_body\_effect\_mismatch\_parameter") unit="sqrt(V)*m"
';
// Diode parameters
parameter real N=1.0 from [1e-6:inf]
  'attr(info="emission\_coefficient")
';
parameter real Is=1e-14 from [1e-20:inf]
  'attr(info="saturation\_current") unit="A"
';
parameter real Bv=100 from [1e-6:inf]
  'attr(info="reverse\_breakdown\_voltage") unit="V"
';
parameter real Ib=1e-3 from [1e-6:inf]
// Local variables
real epsiloni, epsilonox, Thnomk, T2, Tratio, Vto_T, Ucrit_T, Egnom, Eg, Phi_T;
real Weff, Leff, RDeff, RSeff, con1, con2, Vtoa, Kpa, Kpa_T, GammaC, Cepsilon, xi;
real n, deltaV_RSC, Vg, Va, Vd, Vgs, Vgd, Vds, Vs, VG, VS, VD;
real VGprime, VP0, VSprime, VDprime, Gamma0, Gammaprime, Vp;
real n, X1, Iff, X2, ir, Vc, Vds, Vdsprime, deltaV, Vip;
real fl, DeltaL, Lprime, Lmin, Leq, irprime, Beta0, eta;
real Qb0, Beta0prime, nq, Xf, Xr, q0, qS, q1, qB, Beta, Ispecific, Ids, Vib, Idb, Ibb_T;
real A, B, Vt, T2, E_T1, E_T2, Vj_T2, Cj_T2, Fl, F2, F3, Is_T2;
real Id1, Id2, Is1, Is2, Is3, Is4, V1, V2, Ibb_d, Ibb_u, Qd, Qs, Qd1, Qd2, Qs1, Qs2;
real qb, qg, qgso, qgdo, qgbo, fourkt, Sflicker, StoDswap, p_nMOS;

// Equation initialization
p_nMOS = -1.0; // pMOS
A=7.02e-4;
B=1108.0;
epsiloni = 1.0359e-10; // Eqn 4
epsilonox = 3.453143e-11; // Eqn 5
Thnomk = Thnom+273.15; // Eqn 6

// Temperature parameters
T = Ibb / RDeff;

// Local variables
real epsiloni, epsilonox, Thnomk, T2, Tratio, Vto_T, Ucrit_T, Egnom, Eg, Phi_T;
real Weff, Leff, RDeff, RSeff, con1, con2, Vtoa, Kpa, Kpa_T, GammaC, Cepsilon, xi;
real n, deltaV_RSC, Vg, Va, Vd, Vgs, Vgd, Vds, Vs, VG, VS, VD;
real VGprime, VP0, VSprime, VDprime, Gamma0, Gammaprime, Vp;
real n, X1, Iff, X2, ir, Vc, Vds, Vdsprime, deltaV, Vip;
real fl, DeltaL, Lprime, Lmin, Leq, irprime, Beta0, eta;
real Qb0, Beta0prime, nq, Xf, Xr, q0, qS, q1, qB, Beta, Ispecific, Ids, Vib, Idb, Ibb_T;
real A, B, Vt, T2, E_T1, E_T2, Vj_T2, Cj_T2, Fl, F2, F3, Is_T2;
real Id1, Id2, Is1, Is2, Is3, Is4, V1, V2, Ibb_d, Ibb_u, Qd, Qs, Qd1, Qd2, Qs1, Qs2;
real qb, qg, qgso, qgdo, qgbo, fourkt, Sflicker, StoDswap, p_nMOS;

// Equation initialization
p_nMOS = -1.0; // pMOS
A=7.02e-4;
B=1108.0;
epsiloni = 1.0359e-10; // Eqn 4
epsilonox = 3.453143e-11; // Eqn 5
Thnomk = Thnom+273.15; // Eqn 6

// Temperature parameters
T = Ibb / RDeff;
\[ V_{toa} = V_{to} + \frac{A_{to}}{con1} ; \quad //\text{Eqn } 27 \]
\[ K_{pa} = K_p \times (1.0 + A_{kp}/con1) ; \quad //\text{Eqn } 28 \]
\[ K_{pa,T} = K_{pa} \times \text{pow} (\text{Tratio, Bex}) ; \quad //\text{Eqn } 18 \]
\[ C_{epsilon} = 4.0 \times \text{pow} (22 e^{-3}, 2) ; \quad //\text{Eqn } 30 \]
\[ \gamma_0 = \gamma_0 + \frac{A_{\gamma_0}}{con1} ; \quad //\text{Eqn } 29 \]
\[ \xi = 0.028 \times (10.0 \times (L_{eff}/L_k) - 1.0) ; \quad //\text{Eqn } 31 \]
\[ \delta V_{RSCE} = (2.0 \times Q_0/C_{ox}) \times (1.0/\text{pow}(nnn, 2)) ; \quad //\text{Eqn } 32 \]

\[ V_g = p_{n\_MOS} \times V(\text{Gate, Bulk}) ; \]
\[ V_s = p_{n\_MOS} \times V(\text{Source, Bulk}) ; \]
\[ V_d = p_{n\_MOS} \times V(\text{Drain, Bulk}) ; \]
\[ V_g' = V_g - V_{to,T} - \delta V_{RSCE} + \Phi_T + \gamma_0 \times \text{sqrt} (\Phi_T) ; \quad //\text{Eqn } 33 \]

\[ V_{p0} = V_{g'} - \Phi_T \quad //\text{Eqn } 34 \]
\[ V_{p'} = V_{g'} - \Phi_T \quad //\text{Eqn } 35 \]
\[ \xi = (V_p - V_s)/\sqrt{2} ; \quad //\text{Eqn } 36 \]
\[ \gamma_0 = \gamma_0 + \text{sqrt}(V_{p0} + \Phi_T + 4.0 \times \sqrt{2}) ; \quad //\text{Eqn } 37 \]
\[ n = 1.0 + \gamma_0/(2.0 \times \text{sqrt}(V_{p0} + \Phi_T + 4.0 \times \sqrt{2})) ; \quad //\text{Eqn } 38 \]
\[ V_{X1} = \ln (1.0 + \text{limexp}(X1/2.0)) + \ln (1.0 + \text{limexp}(X1/2.0)) ; \quad //\text{Eqn } 39 \]
\[ X2 = (V_p - V_d)/\sqrt{2} ; \]
\[ \text{ir} = \ln (1.0 + \text{limexp}(X2/2.0)) + \ln (1.0 + \text{limexp}(X2/2.0)) ; \quad //\text{Eqn } 35 \]
if (LEVEL == 2)
begin
    Vc = Ucrit_T*Ns*Leff; // Eqn 45
    Vdds = Vc*(sqrt(0.25 + (Vdss/\(Vc\)))*sqrt(iff)) - 0.5; // Eqn 46;
    Vdssprime = Vc*(sqrt(0.25 + (Vdss/\(Vc\)))*sqrt(iff) - 0.75*ln(iff)) - 0.5)
        +Vdss/(2.0+\(Vdt\)) - 0.6 ); // Eqn 47
    if (Lambda+(sqrt(iff) > (Vdss/\(Vdt\)) )
        deltaV = 4.0+\(Vdt\)*sqrt(Lambda*(sqrt(iff) - (Vdss/\(Vdt\))) + (1.0/64.0) ); // Eqn 48
else
    deltaV = 1.0/64.0;
    Vdso2 = (VD-VS)/2.0; // Eqn 49
    Vip = sqrt( pow(Vdss, 2) + pow(deltaV, 2) ) - sqrt( pow(Vdso2-Vdss, 2) )
        + pow(deltaV, 2); // Eqn 50
    Lc = sqrt(Lambda*Lc*ln(1.0+((Vdso2-Vip)/(Leff*Ucrit_T))); // Eqn 51
    Lprime = Ns*Leff - DeltaL + ( (Vdso2+Vip)/Ucrit_T); // Eqn 52
    Lmin = Ns*Leff/10.0; // Eqn 53
    Leq = 0.5*(Lprime + sqrt( pow(Lprime, 2) + pow(Lmin, 2))); // Eqn 54
    X3 = (Vp-Vdso2-VS-sqrt( pow(Vdssprime, 2) + pow(deltaV, 2) )
        + sqrt( pow(Vdso2-Vdssprime, 2) + pow(deltaV, 2))/\(Vdt\);
    irprime = ln((1.0+\(limexp(\(X3/2.0)\)))*ln((1.0+\(limexp(\(X3/2.0)\)))); // Eqn 55
    Beta0 = Kpa_T*(Np*Weff/Leq); // Eqn 56
    eta = 0.3333333; // Eqn 57
    Q0 = Gammaaa*sqrt(Phi_T); // Eqn 58
    Betaprime = Beta0*(1.0 +\(Cox/(\(EO*\epsilonsi)\))*Q0); // Eqn 59
    nq = 1.0 +Gammaaa/2.0*sqrt(Vp+Phi_T+1e-6)); // Eqn 60
end
else
    nq = 1.0 +Gammaaa/2.0*sqrt(Vp+Phi_T+1e-6)); // Eqn 61
//
    Xf = sqrt(0.25+iff); // Eqn 70
    Xr = sqrt(0.25+ir); // Eqn 71
    qD = -nq*( (4.0/15.0)*((3.0*\(pow(Xf,3)\) + 6.0*\(pow(Xf,2)\) + 2.0*\(pow(Xf,1)\)) - 0.5); // Eqn 72
    qS = -nq*( (4.0/15.0)*((3.0*\(pow(Xf,3)\) + 6.0*\(pow(Xf,2)\) + 2.0*\(pow(Xf,1)\)) - 0.5); // Eqn 73
    qI = -nq*( (4.0/3.0)*((pow(Xf,2) + pow(Xr,2))/\(Xf+Xr\)) - 1.0); // Eqn 74
if (LEVEL == 2)
    if (\(VGprime > 0\) )
        qB = (-Gammaaa*sqrt(Vp+Phi_T+1e-6))*1.0/\(Vdt\) - ( (nq-1.0)/nq)*qI; // Eqn 75
    else
        qB = -VGprime/\(Vdt\);
else
    if (\(VGprime > 0\) )
        qB = (-Gammaaa*sqrt(Vp+Phi_T+1e-6))*1.0/\(Vdt\) - ( (nq-1.0)/nq)*qI; // Eqn 75
    else
        qB = -VGprime/\(Vdt\);
//
if (LEVEL == 2)
    Beta = Betaprime/(1.0 +\(Cox/(\(EO*\epsilonsi)\))*\(abs(qB+eta*Iq\)); // Eqn 62
else
    Beta = Kp*(\(Weff/Leff\))/(1+Theta*Vp);
//
    Ispecific = 2.0*n*Beta*\(Vdt\); // Eqn 63
if (LEVEL == 2)
begin
    Ids = Ispecific*(iff-irprime); // Eqn 66
    Vib = VD-VS-ln*2.0*Vdds; // Eqn 67
    if (Vib > 0)
        Idb = Ids*(Iba/Ibb_T)*Vib*exp((-Ibb_T*Lc)/Vib); // Eqn 68
    else
        Idb = 0.0;
end
else

Ids = Ispecific * (iff - ir);  // Eqn 66

// Sthermal = fourkt + Beta*abs(q1);

gm = Beta*$vt*Isqrt( (4.0*iff/Ispecific) + 1.0) - sqrt( (4.0*ir/Ispecific) + 1.0 ) ;
Sflicker = (Kf*gmsgm)/(Np*Weff*Ns*Leff*Cox);

// qB = con2*$vt*qB;

$qg = con2*$vt*(-q1-qB);
$qgso = Cgso*Weff*Np*(VG-VS);
$qgdo = Cgdo*Weff*Np*(VG-VD);
$qgbo = Cgbo*Leff*Np*VG;

// Drain and source diodes
if (StoDswap > 0.0)
begin
V1=p_n_MOS*V(Bulk , Drain_int);
V2=p_n_MOS*V(Bulk , Source_int);
end
else
begin
V2=p_n_MOS*V(Bulk , Drain_int);
V1=p_n_MOS*V(Bulk , Source_int);
end
Id1= (V1>5.0*Np*$vt) ? Area*Is_T2*(limexp( V1/(Np*Vt*T2) ) -1.0) : 0;
Qd1=(V1<Fc+Vj) ? Tt*Id1+Area*(Cj0_T2*Vj/(1-M))*(1-pow((1-V1/Vj*T2),(1-M))): 0;
Id2=(V1<=5.0*Np*$vt) - Area*Is_T2 : 0;
Qd2=(V1>Fc+Vj) ? Tt*Id1+Area*(Cj0_T2*(F1+(1/F2))*(F3*(V1-Fc+Vj*T2)+(M/(2.0*Vj*T2))
+ (V1-Vj-Fc+Vj*T2+Vj*T2))): 0;
Id3=(V1 == -Bv) ? -Ibv : 0 ;
Id4=(V1<=Bv) - Area*Is_T2*(limexp(-(Be+V1)/Vt*T2)-1.0+Bv/Vt*T2) : 0;
Ib_d = Id1+Id2+Id3+Id4;
Qd = Qd1-Qd2;

// Is1= (V2>5.0*Np*$vt) ? Area*Is_T2*(limexp( V2/(Np*Vt*T2) ) -1.0) : 0;
Qs1=(V2<Fc+Vj) ? Tt*Is1+Area*(Cj0_T2*Vj/(1-M))*(1-pow((1-V2/Vj*T2),(1-M))): 0;
Is2=(V2<=5.0*Np*$vt) - Area*Is_T2 : 0;
Qs2=(V2>Fc+Vj) ? Tt*Is1+Area*(Cj0_T2*(F1+(1/F2))*(F3*(V2-Fc+Vj*T2)+(M/(2.0*Vj*T2))
+ (V2-Vj-Fc+Vj*T2+Vj*T2))): 0;
Is3=(V2 == -Bv) ? -Ibv : 0 ;
Is4=(V2<=Bv) - Area*Is_T2*(limexp(-(Be+V2)/Vt*T2)-1.0+Bv/Vt*T2) : 0;
Ib_s = Is1+Is2+Is3+Is4;
Qs = Qs1-Qs2;

// Current contributions
if (StoDswap > 0.0)
begin
if (RDeff > 0.0)
I(Drain_int) = V(Drain , Drain_int)/RDeff;
else
I(Drain_int) = V(Drain , Drain_int)/1e-7;
if (RSelf > 0.0)
I(Source_int) = V(Source , Source_int)/RSelf;
else
I(Source_int) = V(Source , Source_int)/1e-7;
I(Drain_int , Source_int) = p_n_MOS*Ids;
if (LEVEL == 2)
I(Drain_int , Bulk) = p_n_MOS*Ibd;
I(Gate , Drain_int) = p_n_MOS*0.5*ddt(qg);
I(Drain_int , Bulk) = p_n_MOS*0.5*ddt(qb);
I(Source_int , Bulk) = p_n_MOS*0.5*ddt(qb);
I(Gate , Source_int) = p_n_MOS*ddt(qgso);
I(Gate , Drain_int) = p_n_MOS*ddt(qgdo);
I(Gate , Bulk) = p_n_MOS*ddt(qgbo);
I(Bulk , Drain_int) = p_n_MOS*Ibd;
I(Bulk , Drain_int) = p_n_MOS*ddt(Qd);
I(Bulk , Source_int) = p_n_MOS*Ib_s;

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I(Bulk, Source_int) <- p_n_MOS*ddt(Qs);
I(Drain_int, Source_int) <- white_noise(Stermal,"thermal");
I(Drain_int, Source_int) <- flicker_noise(Sflicker, Af, "flicker");
I(Drain, Drain_int) <- white_noise(fourkt/RDeff, "thermal");
I(Source, Source_int) <- white_noise(fourkt/RSeff, "thermal");
end
else
begin
if (RSeff > 0.0)
I(Drain, Drain_int) <- V(Drain, Drain_int)/RSeff;
else
I(Drain, Drain_int) <- V(Drain, Drain_int)/1e-7;
if (RDeff > 0.0)
I(Source, Source_int) <- V(Source, Source_int)/RDeff;
else
I(Source, Source_int) <- V(Source, Source_int)/1e-7;
I(Source_int, Drain_int) <- p_n_MOS*Ids;
if (LEVEL == 2)
I(Source_int, Bulk) <- p_n_MOS*Idb;
I(Gate, Source_int) <- p_n_MOS*0.5*ddt(qg);
I(Gate, Drain_int) <- p_n_MOS*0.5*ddt(qg);
I(Source_int, Bulk) <- p_n_MOS*0.5*ddt(qb);
I(Drain_int, Bulk) <- p_n_MOS*0.5*ddt(qb);
I(Gate, Drain_int) <- p_n_MOS*ddt(qgso);
I(Gate, Source_int) <- p_n_MOS*ddt(ggdo);
I(Gate, Bulk) <- p_n_MOS*ddt(ggbo);
I(Bulk, Source_int) <- p_n_MOS*Ib_d;
I(Bulk, Source_int) <- p_n_MOS*ddt(Qd);
I(Bulk, Drain_int) <- p_n_MOS*Ib_s;
I(Bulk, Drain_int) <- p_n_MOS*ddt(Qs);
I(Source_int, Drain_int) <- white_noise(Stermal,"thermal");
I(Source_int, Drain_int) <- flicker_noise(Sflicker, Af, "flicker");
I(Source_int, Source) <- white_noise(fourkt/RDeff, "thermal");
I(Drain_int, Drain) <- white_noise(fourkt/RSeff, "thermal");
end
end
endmodule
Update number one: September 2008

The first version of the Qucs EPFL-EKV v2.6 model provided Qucs users with reasonably complete long and short channel models for nMOS and pMOS devices. In no respect were these models optimized for minimum simulation run time or were they flexible enough to allow users to select the style of charge partitioning employed by the EKV model. Recent work on the Qucs implementation of the EKV v2.6 MOSFET model and the Qucs ADM-S/XML interface has resulted in a significant reduction in simulation run time overhead, particularly in transient and small signal analysis. The addition of a SPICE BSIM style partition parameter Xpart to the Qucs version of the EKV v2.6 model now allows users to set the style of charge partitioning employed by the EKV model. These notes explain the function of the first EKV v2.6 update and introduce a series of test simulations that demonstrate the effects these changes have on the operation of the Qucs port of the EKV V2.6 model.

Model initialisation

Readers who have looked through the EKV v2.6 Verilog-A code listed in the previous sections of these notes will probably have been struck by the quantity of calculations involved each time the code is evaluated during simulation. In the case of transient analysis it is calculated at least once per time step, often resulting in many thousands of passes through the code. The more MOS devices included in a circuit the greater the time overhead becomes. Obviously, a sensible approach would be to minimize the amount of calculation by only evaluating once those parts of the EKV model equations which result in constant values during simulation. The Verilog-A hardware description language provides a model initialisation feature which selects those parts of a device model code which are to be evaluated prior to the start of a simulation. The resulting calculated variables are then available for use by other sections of the Verilog-A model code during simulation. In transient and small signal analysis this is particularly important as it significantly reduces simulation calculation time. Verilog-A employs the “at” (@(initial_step) or @(initial_model) ) language construction coupled with a begin ... end block to signify the Verilog-A code that is to be evaluated only at model initialisation. Although this technique does greatly improve model simulation speed it does imply significantly more work for the model developer in that the Verilog-A device code has to be split into initialisation and dynamic simulation sections. Readers interested in the detail of how this split can be achieved should compare the latest EKV v2.6 Verilog-A CVS code given at the Qucs Web site with that presented in previous sections of these notes.

Charge partitioning

The MOSFET is a four terminal device with a dynamic performance that requires accurate calculation of the charge at each terminal. Previous notes indicated that the intrinsic channel charge equals the sum of the drain and source charges. However, the exact proportion
of intrinsic channel charge that belongs to the drain or to the source is often not known. The assignment of the proportion of the channel charge to the drain and source charges is called charge partitioning. The first release of the Qucs EKV v2.6 model used the 50/50 partitioning scheme where 50% of the channel charge is arbitrarily assigned to both drain and source. It’s interesting to note that this partitioning scheme has no physical basis but depends entirely on convenience. A second partitioning scheme, called the 40/60 partitioning, does however, have a strong physical basis. Yet a third charge partitioning is often employed for digital circuit simulation; this is known as the 0/100 partition. The second release of the Qucs EPFL-EKV v2.6 model includes an extra parameter called Xpart which allows users to set the partitioning scheme for dynamic simulation calculations. Xpart default is set at 0.4 which corresponds to the 40/60 partitioning scheme. Figure 10 illustrates a test circuit for determining the S-Parameters of an nMOS device connected as a capacitance. Both the device capacitance and associated series resistance can be extracted from S[1,1]. Qucs equation block Eqn1 gives the equations for extracting these properties. Other equations in Eqn1 show how the extracted capacitance can be represented as a ratio of the basic parallel capacitance given by

\[ C_{parallel\_plate} = W \cdot L \cdot Cox. \]  

(30)

Modelling EKV v2.6 charge partitioning using Qucs EDD

Complex simulation results like those shown in Fig 10 suggest the question “How do we check the accuracy of the model being simulated?”. One possible approach is to develop a second model of the same device based on the same physical principles and equations but using a different approach like the Qucs EDD/subcircuit modelling route shown in Fig. 11. It is an EDD/subcircuit model of a long channel EKV v2.6 nMOS device which includes charge partitioning. Figure 12 illustrated the same test circuit as Fig. 10 and the extracted capacitance and resistance values for the EDD model of the long channel nMOS device. A number of features observed from Fig. 10 and Fig. 11 are worth commenting on; firstly that good agreement is recorded between the two sets of results, secondly that the Verilog-A model includes both overlap capacitance and drain and gate source resistances. Hence the slight difference in the capacitance ratio and the recorded values of Rin above one Ohm for the Verilog-A model.

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Figure 10: Test circuit for simulating EKV v2.6 charge partitioning effects: Xpart = 0.4 or QD/QS = 40/60
Figure 11: Qucs EDD model for a EKV v2.6 long channel nMOS device with charge partitioning
Figure 12: Test circuit for simulating EKV v2.6 EDD model charge partitioning effects: Xpart = 0.4 or QD/QS = 40/60
End note

The first update of the Qucs EKV v2.6 model provides users with a more optimised model, with improved simulation performance and a more complete charge partitioning scheme. Even with these changes the model is still not complete. The nMOS and pMOS Verilog-A code needs to be unified and a number of optional parameters need to be added to the Qucs implementation of the EKV v2.6 model. The next update of the model is scheduled for the near future, following correction of bug reports sent in by Qucs users. Once again my thanks to Stefan Jahn for all his help and support during the first EKV v2.6 update development phase.